CLAIMS

What is claimed is:

1. A processor, comprising:

a branch predictor to issue a first branch prediction at a branch location in a program;

a first circuit to detect an exact convergence point subsequent to said branch location in said program;

a scheduler to store instructions of said program subsequent to said branch point when said branch prediction is a misprediction; and

a second circuit to track a first set of physical registers written subsequent to said branch point.

2. The processor of claim 1, wherein said scheduler to re-execute selected instructions of said program subsequent to said branch point.

3. The processor of claim 2, wherein said selected instructions include a first set of instructions of said program whose source physical registers were tracked by said second circuit.

4. The processor of claim 2, wherein said scheduler further executes move instructions corresponding to a second set of instructions that write to said first set of physical registers prior to said exact convergence point.

5. The processor of claim 2, further comprising a recovery buffer to store said selected instructions outside said scheduler.

6. The processor of claim 1, wherein said branch predictor includes a branch target buffer to store target addresses indexed by branch locations in said program and wherein said first circuit includes an alternate target buffer coupled to said branch target buffer for determining said exact convergence point.

7. The processor of claim 6, wherein said branch predictor includes a branch confidence estimator to reverse a second branch prediction of low confidence to induce an induced exact convergence point.

8. The processor of claim 1, wherein said second circuit is a scoreboard including a set of flags corresponding to a set of physical registers, wherein one of said set of flags is set when a corresponding one of said set of physical registers is written between said branch point and said exact convergence point.

9. The processor of claim 8, wherein said one of said set of flags is cleared when said corresponding one of said set of physical registers is written subsequent to said exact convergence point.

10. A method, comprising:

storing a set of instructions of a program subsequent to a mispredicted branch point;

tracking a set of physical registers written by a first selected subset of said set of instructions;

restoring said set of physical registers; and

re-executing a second selected subset of said set of instructions subsequent to an exact convergence point that use a first one of said set of physical registers as a source operand register.

11. The method of claim 10, wherein said tracking includes setting a flag for a second one of said set of physical registers written on a mispredicted path subsequent to said mispredicted branch point.

12. The method of claim 11, further comprising clearing said flag when an instruction subsequent to said exact convergence point uses said second one of said set of physical registers as a source register.

13. The method of claim 10, wherein said storing includes placing said set of instructions in a restore buffer prior to reloading them into a scheduler.

14. The method of claim 10, wherein said restoring includes executing a corresponding move instruction for each of said first selected subset of said set of instructions.

15. The method of claim 10, further comprising reversing a branch prediction of a subsequent branch point to induce said exact convergence point.

16. A system, comprising:

a processor including a branch predictor to issue a first branch prediction at a branch location in a program, a first circuit to detect an exact convergence point subsequent to said branch location in said program, a scheduler to store instructions of said program subsequent to said branch point when said branch prediction is a misprediction, and a second circuit to track a first set of physical registers written subsequent to said branch point;

an interface to couple said processor to input-output devices; and

an audio input-output device coupled to said interface to receive audio data from said processor.

17. The system of claim 16, wherein said scheduler to re-execute selected instructions of said program subsequent to said branch point.

18. The system of claim 17, wherein said selected instructions include a first set of instructions of said program whose source physical registers were tracked by said second circuit.

19. The system of claim 17, wherein said scheduler further executes move instructions corresponding to a second set of instructions that write to said first set of physical registers prior to said exact convergence point.

20. The system of claim 17, further comprising a recovery buffer to store said selected instructions outside said scheduler.

21. The system of claim 16, wherein said branch predictor includes a branch target buffer to store target addresses indexed by branch locations in said program and wherein said first circuit includes an alternate target buffer coupled to said branch target buffer for determining said exact convergence point.

22. The system of claim 21, wherein said branch predictor includes a branch confidence estimator to reverse a second branch prediction of low confidence to induce an induced exact convergence point.

23. The system of claim 16, wherein said second circuit is a scoreboard including a set of flags corresponding to a set of physical registers, wherein one of said set of flags is set when a corresponding one of said set of physical registers is written between said branch point and said exact convergence point.

24. The system of claim 23, wherein said one of said set of flags is cleared when said corresponding one of said set of physical registers is written subsequent to said exact convergence point.

25. An apparatus, comprising:

means for storing a set of instructions of a program subsequent to a mispredicted branch point;

means for tracking a set of physical registers written by a first selected subset of said set of instructions;

means for restoring said set of physical registers; and

means for re-executing a second selected subset of said set of instructions subsequent to an exact convergence point that use a first one of said set of physical registers as a source operand register.

26. The apparatus of claim 25, wherein said means for tracking includes means for setting a flag for a second one of said set of physical registers written on a mispredicted path subsequent to said mispredicted branch point.

27. The apparatus of claim 26, further comprising means for clearing said flag when an instruction subsequent to said exact convergence point uses said second one of said set of physical registers as a source register.

28. The apparatus of claim 25, wherein said means for storing includes means for placing said set of instructions in a restore buffer prior to reloading them into a scheduler.

29. The apparatus of claim 25, wherein said means for restoring includes means for executing a corresponding move instruction for each of said first selected subset of said set of instructions.

30. The apparatus of claim 25, further comprising means for reversing a branch prediction of a subsequent branch point to induce said exact convergence point.